

Fig. 1 (Prior Art)

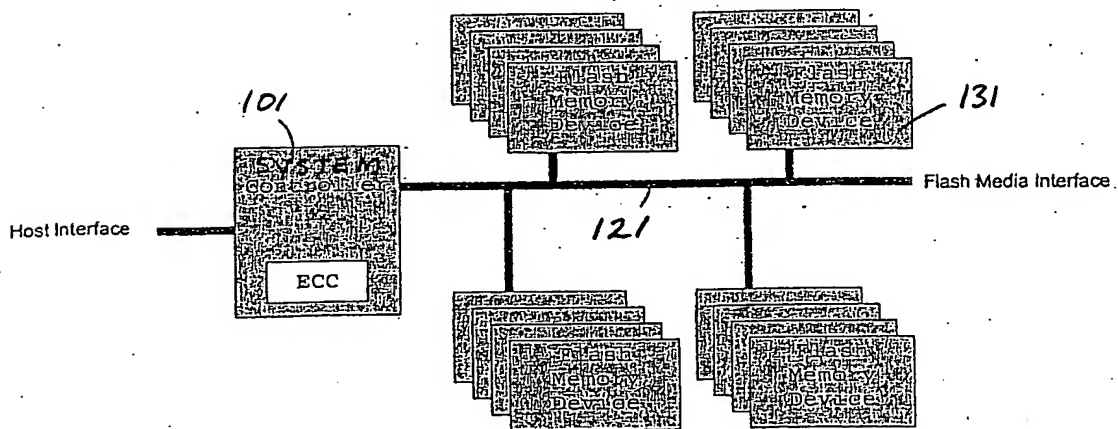


Fig. 2 (Prior Art)

10081375.022202

2022051800T

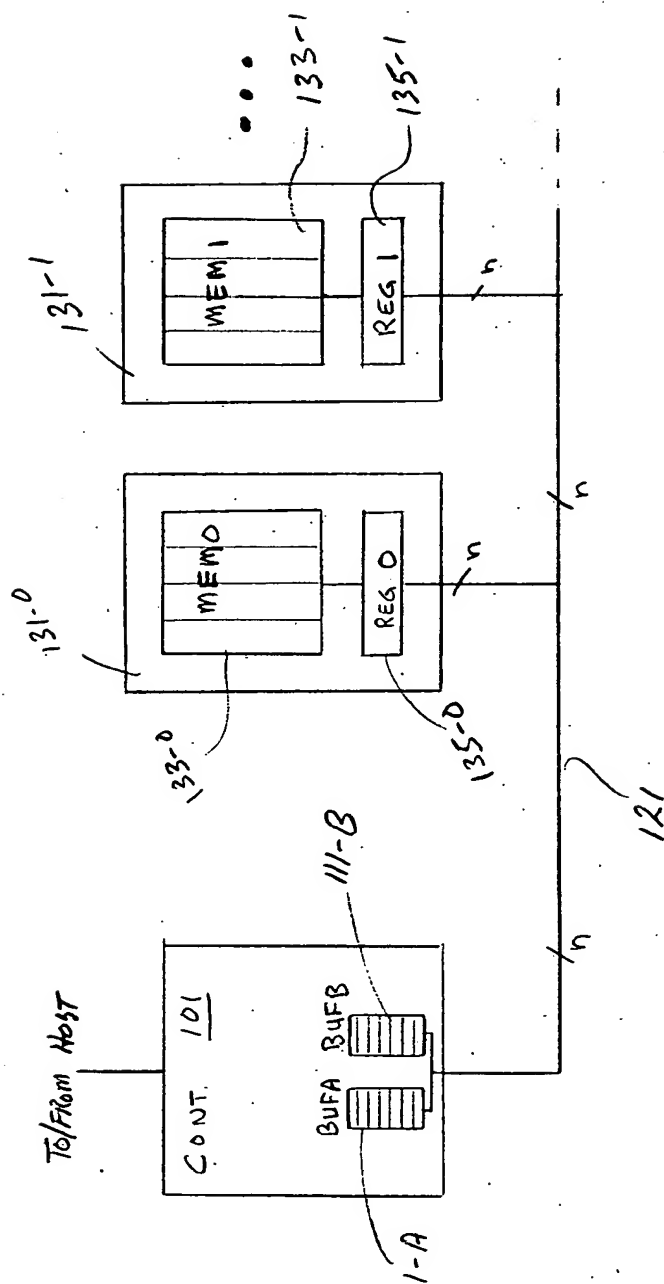
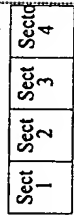


Figure 3

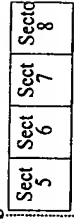
202220" SETBOOT

Controller

Buffer A Transfers
(host to controller)



Buffer B Transfers
(host to controller)



Memory 0

Data Transfers
(controller to memory)
Program Operations
(in memory)

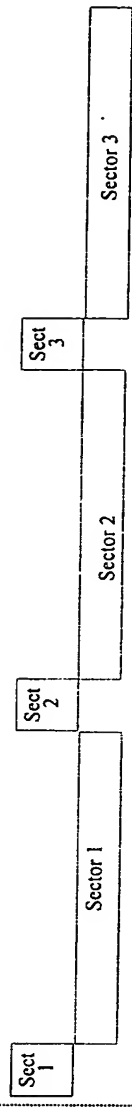


Figure 4A

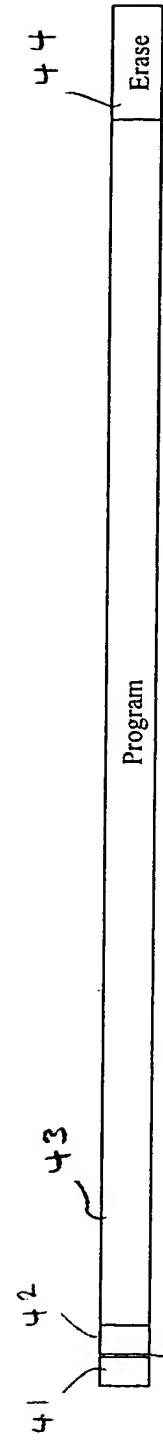


Figure 4B

Controller

Buffer A Transfers
(host to controller)

Sect 1	Sect 2	Sect 3	Sect 4
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Buffer B Transfers
(host to controller)

Sect 5	Sect 6	Sect 7	Sect 8
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Memory 0

(controller to memory)
Data Transfer

Sect 1	Sect 2	Sect 3	Sect 4
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PROGRAM
Operations
(in memory)

Sector 1
Sector 2
Sector 3
Sector 4

Sect 5	Sect 6	Sect 7	Sect 8
--------	--------	--------	--------

Sector 5
Sector 6
Sector 7
Sector 8

Sect 9	Sect 10	Sect 11	Sect 12
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Figure 5B

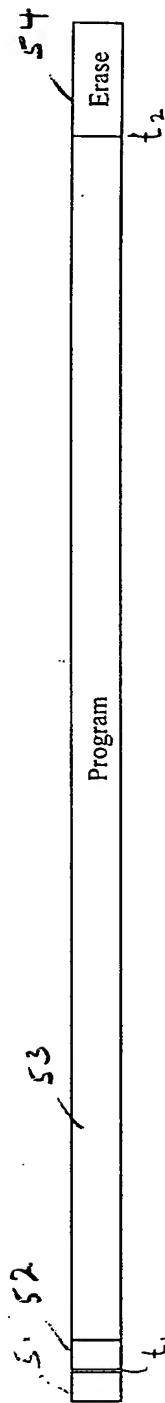


Figure 5B

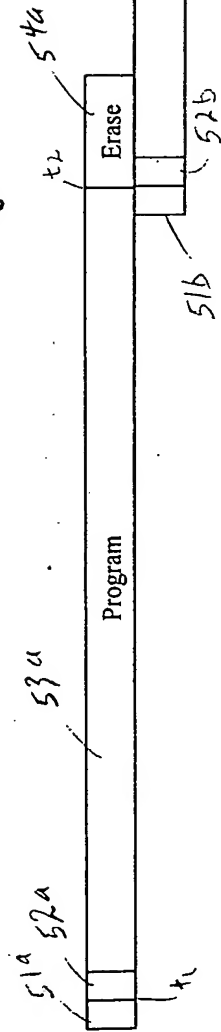


Figure 5C

202220" S/E T800T

Controller

Buffer A Transfers (host to controller)

Sect 1	Sect 2	Sect 3	Sect 4
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Buffer B Transfers

(host to controller)

Sect 5	Sect 6	Sect 7	Sect 8
--------	--------	--------	--------

Memory 0

(Controller to memory)
Data Transfer

Sect 1	Sect 2	Sect 3	Sect 4
--------	--------	--------	--------

Program

Operations

(in memory)

Sector 1
Sector 2
Sector 3
Sector 4

Memory 1

(Controller to memory)
Data Transfer

Sect 5	Sect 6	Sect 7	Sect 8
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Program

Operations

(in memory)

Sector 5
Sector 6
Sector 7
Sector 8

Sect 9	Sect 10	Sect 11	Sect 12
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Sect 13	Sect 14	Sect 15	Sect 16
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Sect 9	Sect 10	Sect 11	Sect 12
--------	---------	---------	---------

Sector 9
Sector 10
Sector 11
Sector 12

Sect 13	Sect 14	Sect 15	Sect 16
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Sector 13
Sector 14
Sector 15
Sector 16

t_1

t_2

t_3

t_4

t_5

Figure 4A

